

(An ISO 3297: 2007 Certified Organization) Vol. 5, Issue 7, July 2016

A 4.7 nA, 1.2V, CMOS Current Reference Circuits Using Sub-threshold Operation

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ABSTRACT: A low-power CMOS current reference circuit operating with a supply voltage ranging from 1.2V to 1.8V has been implemented in 0.18 UMC CMOS process, providing a mean reference current of 4.7nA.The device consists of MOSFET circuits operated in the saturation and sub-threshold region and uses no resistors. Accurate sub-threshold design allows the circuit to work at room temperature with supply voltage 1.2V. The average temperature coefficient measured from -40° C to 80° C is 854ppm/ $^{\circ}$ C and the line regulation is 0.9%/V.

KEYWORDS: complementary metal-oxide semiconductor (CMOS), current reference, power-aware large-scale integrations(LSIs),self-biasing circuit,subthreshold region, temperature dependence, ultralow power,weak inversion..

I. INTRODUCTION

Current reference circuits are important building blocks for analog and mixed-signal circuit systems in microelectronics. they are indispensible components for producing reference current for various analog circuits, such as operational amplifiers, analog buffers, oscillators, and analog-to-digital/digital-to-analog converters. Nano ampere current reference have been strongly desired particularly for use in ultralow-power large-scale integration(LSI) applications. such as radio frequency identifications(RFIDs), implantable medical devices, and smart sensor networks.these LSIs have to operate with ultralow power ,e.g., a few microwatts or less, because they will probably be placed under conditions where they will rely on poor energy sources, such as microbatteries and energy-harvesting devices.because the power dissipation and performance of these circuits are determined mainly by their bias currents, current reference with nanoampere-order currents are required to ensure stable and highly precise circuit operation

Nanoampere current reference have been reported in several papers. however their power dissipation are still large and their output currents have a large positive temperature dependence. this is unsuitable for practical applications.the current reference circuit that we designed will solve this problem and can be used for ultralow-power LSIs.our circuit consists of MOSFET circuits operating in the subthreshold region with operation of a few microwatts and no resistor.it can provide a reference current that is insensitive to temperature and supply voltage.



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

II. RELATED WORK

Reference [1] shows a current reference circuit with a $1.4\mu W 24.9ppm^{0}C$ current reference with process insensitive temperature compensation in 0.18µm CMOS. The proposed circuit employs ratio between the process independent temperature coefficients of resistor and and comensation voltage.it consumes 1.4µW from 1-v supply.it acchives temperature coefficient of 24.9 ppm/⁰C with 0⁰C to 100⁰C. Reference [2] is A Resistor-free Temperature Compensated CMOS current reference The proposed circuit is implemented 0.18µm CMOS standard technology and operates with supply voltage in the range of 2V to 2.8V from $-25^{\circ}/\text{C}$ to $130^{\circ}/\text{C}$.the reference current is $1\mu\text{A} \pm 1\text{nA}$ has a temperature coefficient of 12.9 ppm/⁰C and a line sensitivity of 8.7 nA/V.. Reference [3] is A 2.6nW,0.45V Temperature Compensated Subtreshold CMOS Voltage reference circuit shows a voltage reference circuit operating with all transistor biased in weak inversion providing a mean reference voltage of 257.5 mV has been fabricated in 0.18µm CMOS standard technology.accurate subthreshold design allows subthreshold design allow the circuit to work at room temperature with supply voltage down to 0.45V and an average current consumption 5.8 nA and an average temperature coefficient of 165 ppm/ $^{\circ}$ C with a standard deviation of 100 $^{\circ}$ C in a temperature range from 0 $^{\circ}$ C to 125 $^{\circ}$ C. Reference [4] is A CMOS Sub 1-V nano power current and voltage reference with leakage compensation.in this paper a CMOS Sub-1-V nanopower reference is proposed which is implemented without resistors and only CMOS transistors.the proposed circuit has most attractive merit that it can afford reference current and voltage simultaneously. moreover the leakage compensation technique is utilized, and thus it has a very low temperature for wide temperature range.the proposed circuit is verified by SPICE simulation with a 0.18µm CMOS standard technology. The temperature coefficient of reference voltage and reference current are 0.0037%/°C AND 0.0091%/°C, respectively also the power supply voltage can be as low as 0.85V and its power consumption is only5.1 nW.

III. CIRCUIT DESIGN

Fig.1 shows our current reference circuit .the circuit consists of a bias-voltage subcircuit is a modified \hat{a} multiplier self biasing circuit that uses a MOS resistor M3,instead of ordinary resistors. Bias voltage V_B for mos resistor M3 is generated by a diode-connected transistors M4.the current-source subcircuit accepts bias voltage V_B and generates reference current I_{OUT} that is independent of temperature and supply voltage .All MOSFET are operated in the subthreshold region, except for M3 and M4.A start-up cicuit is required to avoid the stable state in the zero bias condition.

The bias-voltage subcircuit is divided into three components.thsese components as follows:

- 1) â multiplier self-biasing circuit with MOS resistor.
- 2) diode-connected transistor(M_{4})
- 3) p-channel operate MOS current mirror

The subthreshold drain current I_D of a MOSFET is an exponential function of the gate-source voltage V_{GS} and the drain-source voltage V_{DS} , and is given by

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$
$$I_0 = \mu C_{OX} (\eta - 1) V_T^2$$

Where K is the aspect ratio (W/L) of the transistor, μ is the carrier mobility, Cox is the gate-oxide capacitance, V_T (= $k_B T/q$) is the thermal voltage, K_B is the Boltzmann constant, T is the Temperature, q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor.for $V_{DS} > 0.1$ V, current I_D is almost independent of V_{DS} and given by



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)$$



Fig. 1. Circuit Diagram of Proposed Current Reference circuit.

IV. EXPERIMENTAL RESULTS

SPICE simulation were carried out to evaluated the performance of the proposed circuit design for a 180nm with a supply voltage of 1.2V to 1.8V.



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016



Fig2.Simultaed output current Iref at room temperature as function of suplly voltage

Fig 2 shows the supply voltage dependence of the output reference current Iref at room temperature. The power supply voltage was set in the range of 1.2V to 1.8V the output current was about 4.75 nA and almost constant at room temperature in the range of -40° C TO 80° C the temperature coefficient is 854 ppm/ $^{\circ}$ C respectively. almost a constant reference current was obtained over a wide temperature range.



Fig3.measured output cuurent Iref as a function of temperature, with various supply voltage



(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

Fig 3.shows the measured output current at different temperature range from -40° C to $+80^{\circ}$ C. The power supply voltage was set in the range of 1.2V to 1.8V.when V_{DS}>0.1 current Iref is almost independent of V_{DS} and is given by



$$I_D = KI_0 \exp \left(\frac{V_{GS} - V_{TH}}{\eta V_T} \right)$$

Fig 4.measured output current Iref at different temperature.

Fig 4.shows measured output current as a function of temperature.range from -40° C to 80° C with a temperature coefficient of 854PPM/ $^{\circ}$ C.and line sensitivity is 0.9%/V.



Fig 5. Measured output power

Fig 5.shows the total output power at room temperature with a supply voltage of 1.2V.



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Vol. 5, Issue 7, July 2016

TABLE PERFORMANCE COMPARISON OF THIS WORK WITH RECENTLY PUBLISHED CURRENT REFRENCE CIRCUIT

	This work	[4]	[5]	[6]	[7]
Technology(µm)	0.18	0.18	0.18	0.35	0.18
Temperature Range(⁰ C)	-40 to 80	0-100	-20 - 120	0-80	-20 - 80
Supply Voltage(V)	1.2-1.8	.45-2	0.85-2.5	1.8 – 3V	1.4-3
l _{ref(nA)}	4.7nA	7810nA	10000nA	96nA	36
TC(ppm/ ⁰ C)	854	24.9	170	520	2200
Line Sensitivity(ppm/V)	900	1300	3000	200	2000
Power(nw)	183.45	1400	8000	1000	3000

V. CONCLUSION

We have developed an ultralow-power CMOS current reference circuit consisting of subthreshold MOSFET circuit and no resistors the device generates a temperature and supply voltage compensated reference current.our circuit generates a 4.715nA output current the temperature coefficient and ine regulation of the output current were 854ppm/⁰C and 0.9%/V, respectively the power dissipation was about 0.18μ W.our circuit will be useful as a current reference circuit for use in power-aware LSI applications, such as RFIDs, implantable medical devices, and smart sensor network.

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